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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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10/551,702

09/30/2005

Haruki Toda

89165.0025

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26021 7590 06/15/2007

HOGAN & HARTSON L.L.P.
1999 AVENUE OF THE STARS
SUITE 1400
LOS ANGELES, CA 90067

EXAMINER

VALENTINE, JAMI M

ART UNIT

PAPER NUMBER

2815

MAIL DATE

DELIVERY MODE

06/15/2007

PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No. 10/551,702	Applicant(s) TODA, HARUKI	
	Examiner Jami M. Valentine, Ph.D.	Art Unit 2815	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 30 September 2005.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-23 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-23 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☒ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 30 September 2005 is/are: a) ☐ accepted or b) ☒ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08)
Paper No(s)/Mail Date <u>9/30/05</u> . | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

Status of the Application

1. **Claims 1-23** are pending in this application.

US National Phase of PCT

2. Acknowledgment is made that this application is the US national phase of international application PCT/JP03/04275 filed 3 April 2003 which designated the U.S.

Foreign Priority

3. Acknowledgment is made that the certified copy of the foreign priority document has been received in the national stage application from the International Bureau.

Information Disclosure Statement

4. Acknowledgment is made that the information disclosure statement has been received and considered by the examiner. If the applicant is aware of any prior art or any other co-pending applications not already of record, he/she is reminded of his/her duty under 37 CFR 1.56 to disclose the same.

Drawings

5. The drawings are objected to because figures 1, 3-6, 11-13, 17B, 18 and 22 are informal. It appears that these figures were printed on a faulty printer, as these figures are faded. Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is

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being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Specification

6. The abstract of the disclosure is objected to because it has too many words. The abstract must contain 50 –150 words. Correction is required. See MPEP § 608.01(b).
7. The disclosure is objected to because of the following informalities: repeated instances of poor grammar, misspellings, and sentence construction, e.g. paragraphs [0003], [0005], [0035] and [0037]. Appropriate correction is required.
8. The listing of references in the specification (e.g. [0004]) is not a proper information disclosure statement. 37 CFR 1.98(b) requires a list of all patents, publications, or other information submitted for consideration by the Office, and MPEP § 609.04(a) states, "the list may not be incorporated into the specification but must be submitted in a separate paper." Therefore, unless the references have been cited by the examiner on form PTO-892, they have not been considered.

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Claim Objections

9. Claim 9 is objected to because of the following informalities: There is a grammatical error: "...thereby simultaneously accessing to the respective plural memory cells..."

Appropriate correction is required.

Claim Rejections - 35 USC § 112

10. The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

11. **Claims 15-23** are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

12. **Per Claim 15**, the following language is indefinite: "...a prespecified pitch..." It is unclear what is meant by a prespecified pitch. Any pitch is a prespecified pitch. Hence, one of ordinary skill in the art would not be reasonably apprised of the scope of the invention and this claim is rendered indefinite.

Claim Rejections - 35 USC § 102

13. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

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14. **Claims 1-7** are rejected under 35 U.S.C. 102(b) as being anticipated by Ovshinsky et al. (US Patent No 6,141,241) hereinafter referred to as Ovshinsky.

15. Per **Claim 1** Ovshinsky discloses a phase change memory device, comprising

- a semiconductor substrate (column 13, line 4)
- a plurality of cell arrays stacked above said semiconductor substrate, each cell array having memory cells arranged in a matrix manner (see figure 9)
- bit lines (10) each commonly connecting one ends of plural memory cells arranged in a first direction of said matrix. (see figure 9)
- and word lines (12) each commonly connecting the other ends of plural memory cells arranged in a second direction of said matrix; (see figure 9)
- a read/write circuit formed on said semiconductor substrate as underlying said cell arrays for reading and writing data of said cell arrays; (column 7 lines 52-57)
- first and second vertical wirings disposed outside of first and second boundaries that define a cell layout region of said cell arrays in said first direction to connect said bit lines of the respective cell arrays to said read/write circuit; and third vertical wirings disposed outside of one of third and fourth boundaries that define said cell layout region in said second direction to connect said word lines of the respective cell arrays to said read/write circuit. (column 19 lines 8-12; figure 9)

16. Additionally, claim 1 recites the performance properties of the device (e.g. storing resistance values as data that are determined by phase change of said memory cells). This functional limitation does not distinguish the claimed device over the prior art, since it appears that this limitation can be performed by the prior art structure of Ovshinsky. While features of

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an apparatus may be recited either structurally or functionally, claims directed to an apparatus must be distinguished from the prior art in terms of structure rather than function. In re Schreiber, 128 F.3d 1473, 1477-78, 44 USPQ2d 1429,1431-32 (Fed. Cir. 1997) See MPEP 2114.

17. Per **Claim 2**, Ovshinsky discloses the device of claim 1, including where each said memory cell has a stack structure of a chalcogenide and a diode as disposed at each cross portion of said bit lines and word lines in the respective cell arrays. (column 18, lines 37-48)

18. Per **Claim 3**, Ovshinsky discloses the device of claim 2, including where said diode of said memory cell is serially connected to said chalcogenide while having a polarity with said bit line side as a cathode and with said word line side as an anode (e.g. figure 9)

19. Additionally, claim 3 recites the performance properties of the device (e.g wherein said bit lines and word lines are so potentially fixed as to reversely bias said diode in a non-selected mode...). This functional limitation does not distinguish the claimed device over the prior art, since it appears that this limitation can be performed by the prior art structure of Ovshinsky.

While features of an apparatus may be recited either structurally or functionally, claims directed to an apparatus must be distinguished from the prior art in terms of structure rather than function. In re Schreiber, 128 F.3d 1473, 1477-78, 44 USPQ2d 1429,1431-32 (Fed. Cir. 1997) See MPEP 2114.

20. Per **Claim 4**, Ovshinsky discloses the device of claim 1, including where each said cell arrays are so stacked as to share bit lines (10) and word lines (12) with adjacent two cell arrays. (e.g. figure 9)

21. Per **Claim 5**, Ovshinsky discloses the device of claim 1, including where said first to third vertical wirings are contact plugs which are buried in an interlayer dielectric film

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surrounding said cell arrays. The examiner takes official note of the equivalence of contact plugs and vertical vias. (Gardner US Patent No 5,955,785 is provided as a teaching reference).

22. Per **Claims 6-7**, Ovshinsky discloses the device of claim 1, including where neighboring two memory cells in each said cell array constitute a pair cell for storing complementary data. Additionally, claim 6 recites the performance properties of the device. This functional limitation does not distinguish the claimed device over the prior art, since it appears that this limitation can be performed by the prior art structure of Ovshinsky. While features of an apparatus may be recited either structurally or functionally, claims directed to an apparatus must be distinguished from the prior art in terms of structure rather than function. In re Schreiber, 128 F.3d 1473, 1477-78, 44 USPQ2d 1429,1431-32 (Fed. Cir. 1997) See MPEP 2114.

Claim Rejections - 35 USC § 103

23. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

24. **Claims 15-17** is rejected under 35 U.S.C. 103(a) as being unpatentable over Ovshinsky.

25. Per **Claim 15**, Ovshinsky discloses the device of claim 1.

26. The limitations of claim 15 would have been obvious to one having ordinary skill in the art at the time the invention was made since it has been held that mere duplication of the essential working parts of a device involves only routine skill in the art. *St. Regis Paper Co. v. Bemis Co.*, 103 USPQ 8.

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27. Per **Claim 16**, Ovshinsky discloses the device of claim 15, including where each said memory cell has a stack structure of a chalcogenide and a diode as disposed at each cross portion of said bit lines and word lines in the respective cell arrays. (column 18, lines 37-48)

28. Per **Claim 17**, the limitations are "product-by-process" limitations. While product-by-process claims are limited by and defined by the process, determination of patentability is based on the product itself. In re Hirao, 190 USPQ 15 at 17(footnote 3). The patentability of a product does not depend on its method of production. If the product in the product-by-process claim is the same as or obvious from a product of the prior art, the claim is unpatentable even though the prior product was made by a different process. *In re Thorpe*, 777 F.2d 695, 698, 227 USPQ 964, 966 (Fed. Cir. 1985) See also in re Brown, 173 USPQ 685; In re Luck, 177 USPQ 523; In re Fessmann, 180 USPQ 324; In re Avery, 186 USPQ 116 in re Wertheim, 191 USPQ 90 (209 USPQ 254 does not deal with this issue); and In re Marosi et al, 218 USPQ 289 final product per se which must be determined in a "product by, all of" claim, and not the patentability of the process, and that an old or obvious product, whether claimed in "product by process" claims or not. Note that Applicant has the burden of proof in such cases, as the above case law makes clear.

29. **Claims 8-14 and 18-23** are rejected under 35 U.S.C. 103(a) as being unpatentable over Ovshinsky in view of D.C. McClure (US Patent No 5,657,292) hereinafter referred to as McClure.

30. Per **Claims 8 and 18** Ovshinsky discloses the device of claim 1, but fails to teach the limitations of claim 8.

31. McClure teaches a read/write circuit including

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- said read/write circuit comprises: a global bus region having a plurality of data lines to which read data are transferred and a plurality of write pulse signal lines for transferring write pulses to said bit lines, (figure 6D)
- said data lines and said write pulse signal lines being so disposed as to cross a central portion of said cell layout region in said second direction; first and second bit line select circuits disposed along said first and second boundaries of said cell layout region, respectively, to which the respective bit lines of neighboring two cell arrays are connected; (column 3 lines 60-66)
- first and second sense amp arrays for sensing data of bit lines selected by said first and second bit line select circuits, respectively, said first and second sense amp arrays being disposed between said first, second bit line select circuits and said global bus region, respectively; (figure 6D)
- a word line select circuit disposed along one of said third and fourth boundaries of said cell layout region, to which shared word lines of said neighboring two cell arrays are connected; (column 5 lines 1-17)
- a write circuit disposed along the other of said third and fourth boundaries of said cell layout region for generating said write pulses supplied to said write pulse signal lines. (figures 9-10)

32. It would have been obvious to one having ordinary skill in the art at the time the invention was made to combine the circuit of McClure with the device of Ovshinsky, and the motivation to do so would have been primarily to take advantage of existing technology, and

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secondarily, in order to provide a fast circuit (McClure, column 2 lines 59-61) as the addressing matrix (column 21, lines 7-16)

33. Per **Claims 9-12, 19-23** recite functional limitations. This functional limitation does not distinguish the claimed device over the prior art, since it appears that this limitation can be performed by the prior art structure of Ovshinsky in view of McClure. While features of an apparatus may be recited either structurally or functionally, claims directed to an apparatus must be distinguished from the prior art in terms of structure rather than function. In re Schreiber, 128 F.3d 1473, 1477-78, 44 USPQ2d 1429,1431-32 (Fed. Cir. 1997) See MPEP 2114.

34. Per **Claims 13-14**, Ovshinsky in view of McClure teach the device of claim 8, including a write circuit, a logic pulse generation circuit and a write pulse generation circuit. The limitations of claims 13 and 14 would have been obvious to one having ordinary skill in the art at the time the invention was made, since it appears that these limitations can be performed by the prior art structure of Ovshinsky in view of McClure.

Cited Prior Art

35. The following prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Reference 1: US Patent No 5,955,785 by Gardner et al. is cited as a teaching reference.

Reference 2: US Patent No 6,351,427 by Brown et al.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jami M. Valentine, Ph.D. whose telephone number is (571) 272-

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9786. The examiner can normally be reached on Mon-Thurs 8:30am-7pm EST. **NOTE:** From June 18 through August 8th, The examiner will be available *only* on Thursdays and Fridays 8:30am-7pm EDT, due to jury duty service.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kenneth Parker can be reached on (571) 272-2298. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Jami M Valentine, Ph.D.
Examiner
Art Unit 2815

JMV


JEROME JACKSON
PRIMARY EXAMINER